

Enseignes et afficheurs à LED

Circuits logiques programmables : FPGA



Dr. Mamadou Lamine NDIAYE

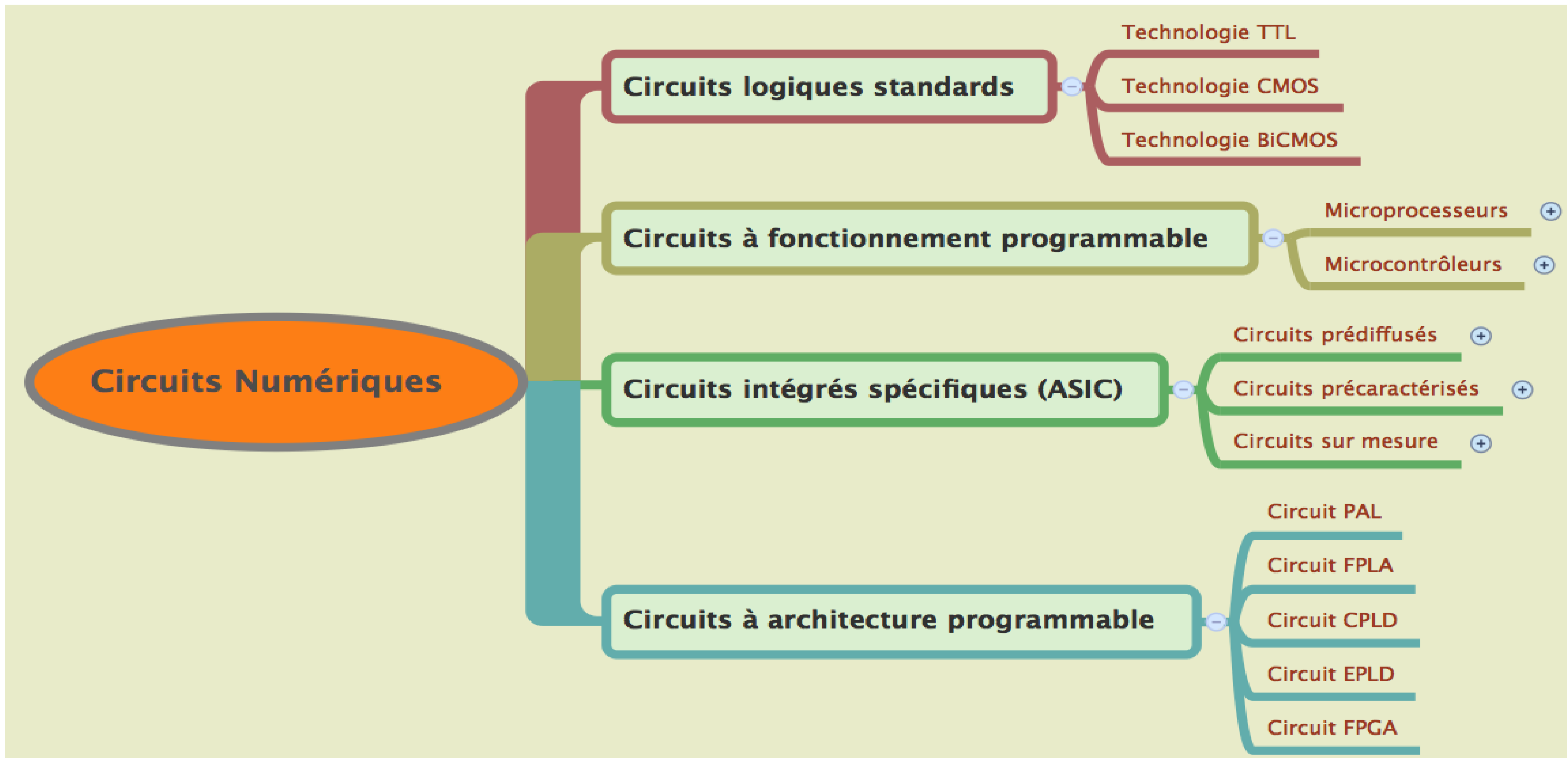
Circuits logiques programmables : FPGA



Mamadou Lamine NDIAYE

- Les circuits logiques programmables
- Les circuits FPGA
- Méthodologie de conception des circuits FPGA
- Environnement de développement

Classification des circuits logiques

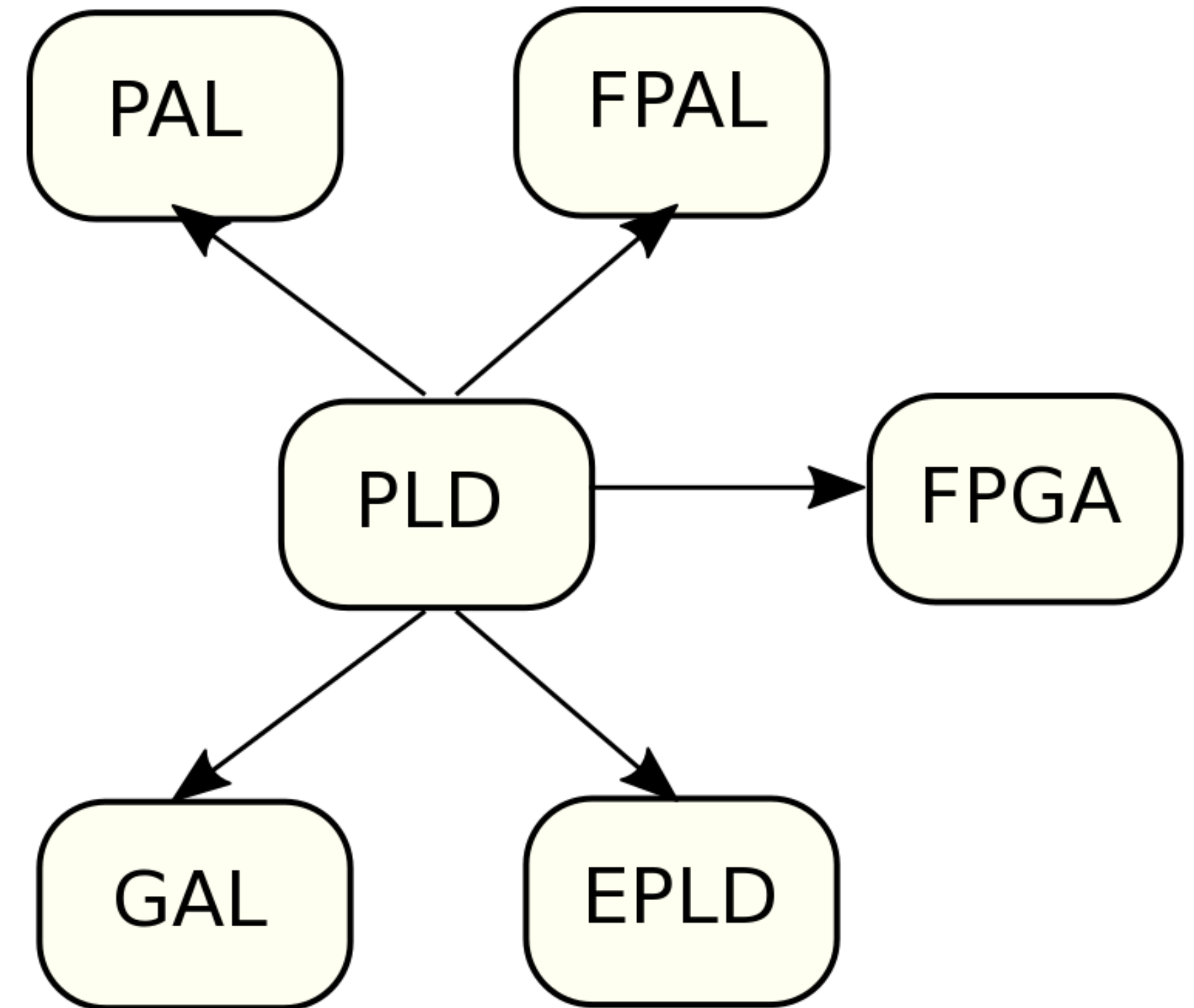


Circuits logiques programmables



Ensemble de portes logiques reconfigurables

- ET, OU
- Bascules, RAM, Multiplexeurs, registres



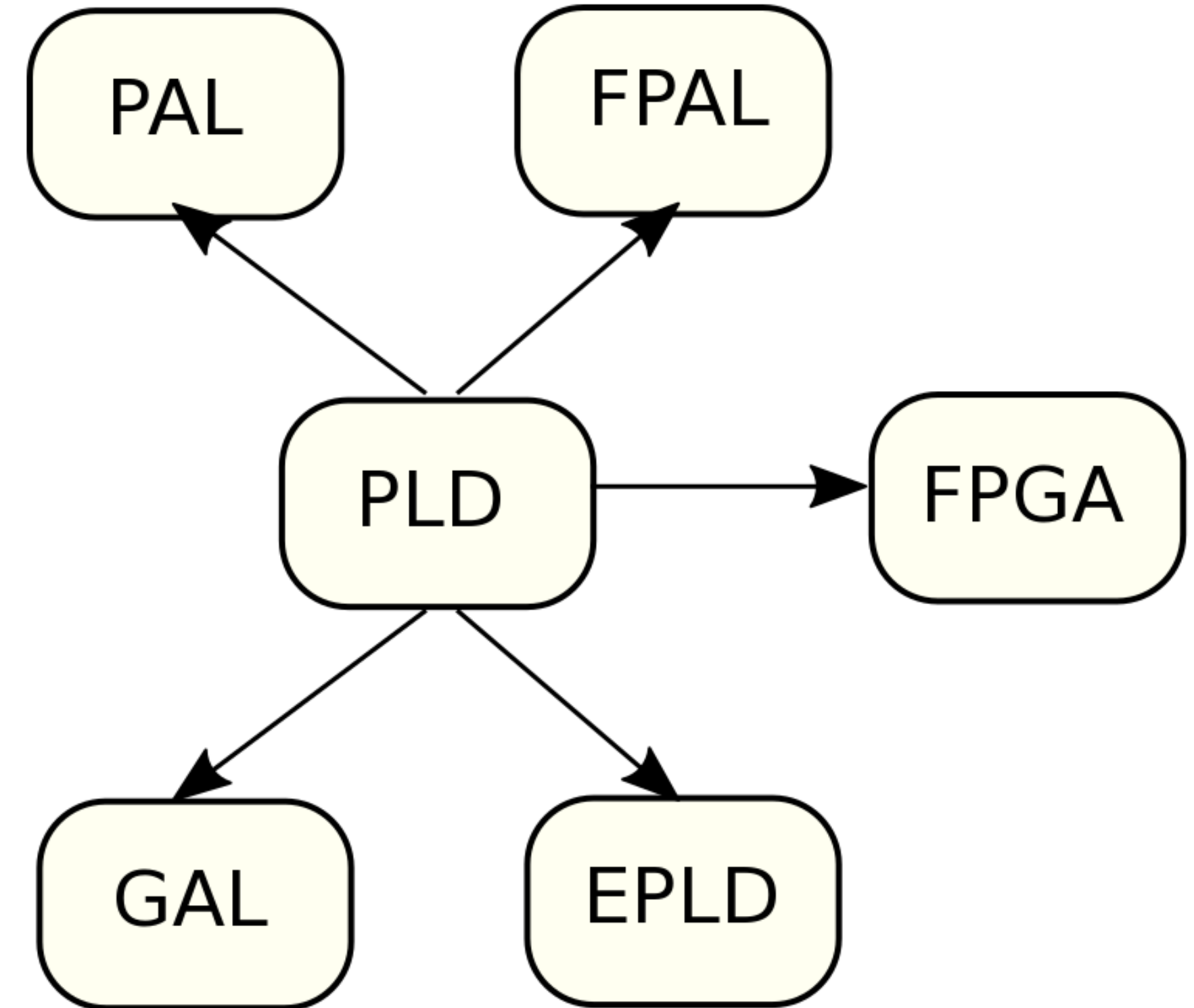
Circuits logiques programmables



Ensemble de portes logiques reconfigurables

- ET, OU
- Bascules, RAM, Multiplexeurs, registres

- Technologies fusible,
- Technologies Flash, EEPROM, SRAM



- Circuit PAL (Programmable Array Logic) où seules les fonctions ET sont programmables
- Circuit FPLA (Field Programmable Logic Array) est un circuit PAL dans lequel les fonctions ET et OU sont programmables
- Circuit CPLD (Complex Programmable Logic Device) est un circuit logique programmable complexe
- Circuit EPLD (Erasable Programmable Logic Device) est un circuit logique programmable et effaçable
- Circuit FPGA (Field Programmable Gate Array) est un réseau de circuits programmables à la demande

Les circuits FPGA



- Les circuits logiques programmables de type FPGA sont de plus en plus utilisés dans la conception des circuits numériques.
 - Matrices de fonctions logiques (cellules logiques SRAM)
 - Programmation des interconnexions (reconfiguration de l'architecture) in situ
 - Reprogrammables à volonté
 - Temps de développement très court.
 - Grande souplesse pour des évolutions rapides à moindre coût

- Les circuits logiques programmables de type FPGA sont de plus en plus utilisés dans la conception des circuits numériques.
 - Densités d'intégration pouvant atteindre plus de 10 millions de portes logiques.
 - Possibilités de traitement parallèle des données (augmentation de la vitesse de calcul).
 - Blocs logiques configurables constitués d'arbres de multiplexeurs connectés à des points mémoires.
 - Capacité limitée par le nombre de blocs logiques configurables (non la complexité).

Niveaux de description

● Comportemental ou fonctionnel

- Le modèle est décrit par, sa fonction, son algorithme. Il s'agit de décrire comment cela fonctionne.

● RTL (Register Transfert Logic)

- Le modèle est décrit sous forme d'éléments séquentiels
- Prend en compte la notion d'horloge, de cycle;

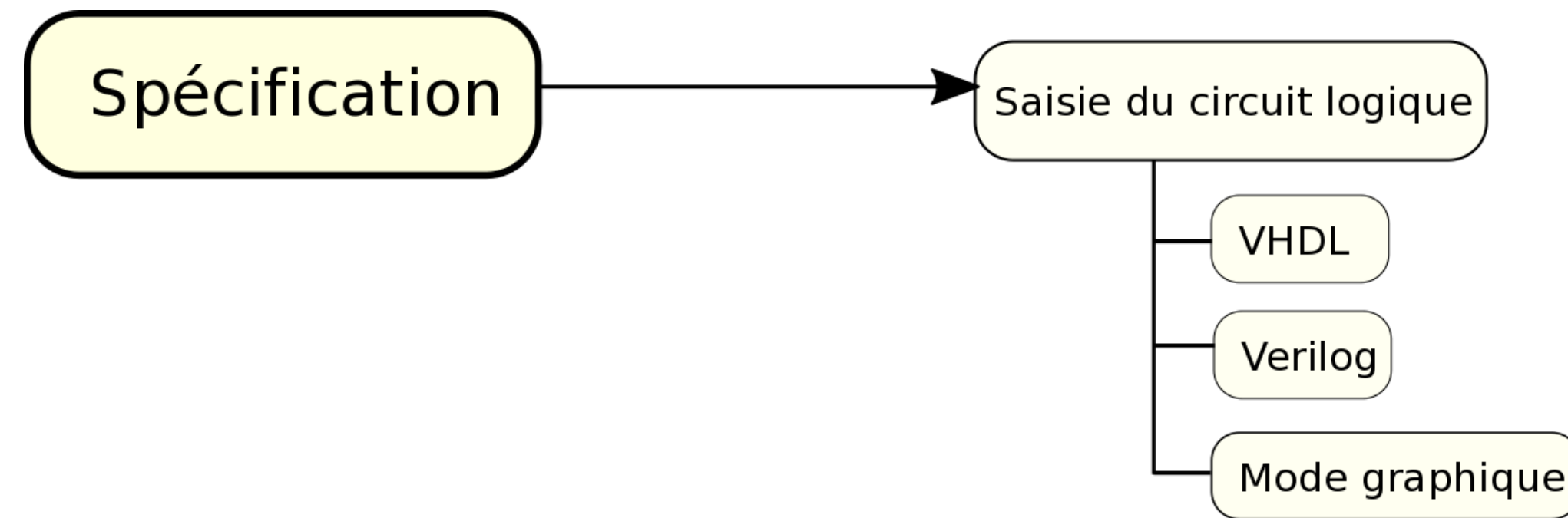
● Structurel (Porte logique)

- Le modèle est décrit par sa topologie (netlist) de portes logiques, de registres, de composants

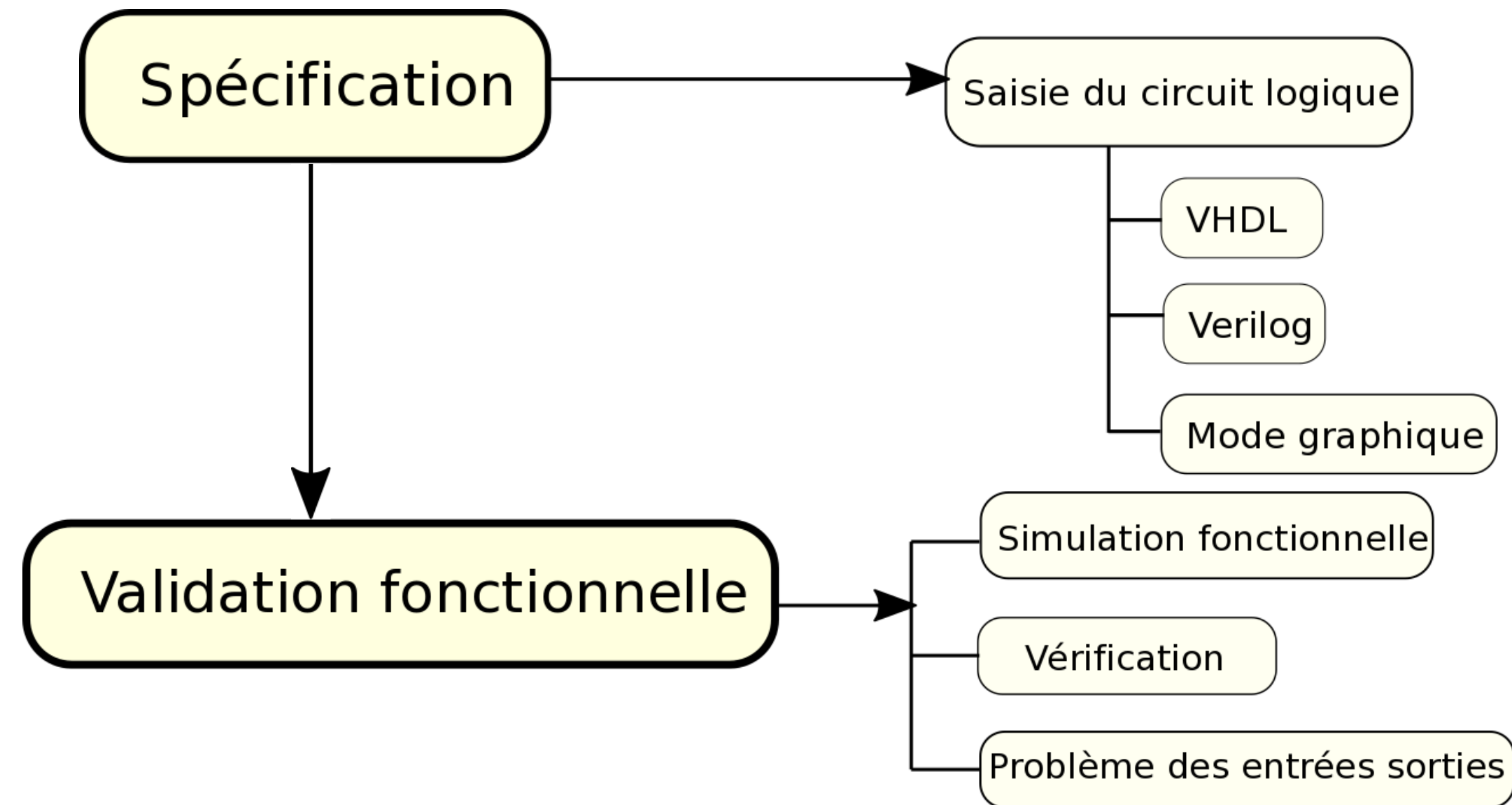
● Décomposition du cahier des charges en fonctions simples

- Fonctions combinatoires (**instructions concurrentes**)
- Fonctions séquentielles (**process**)

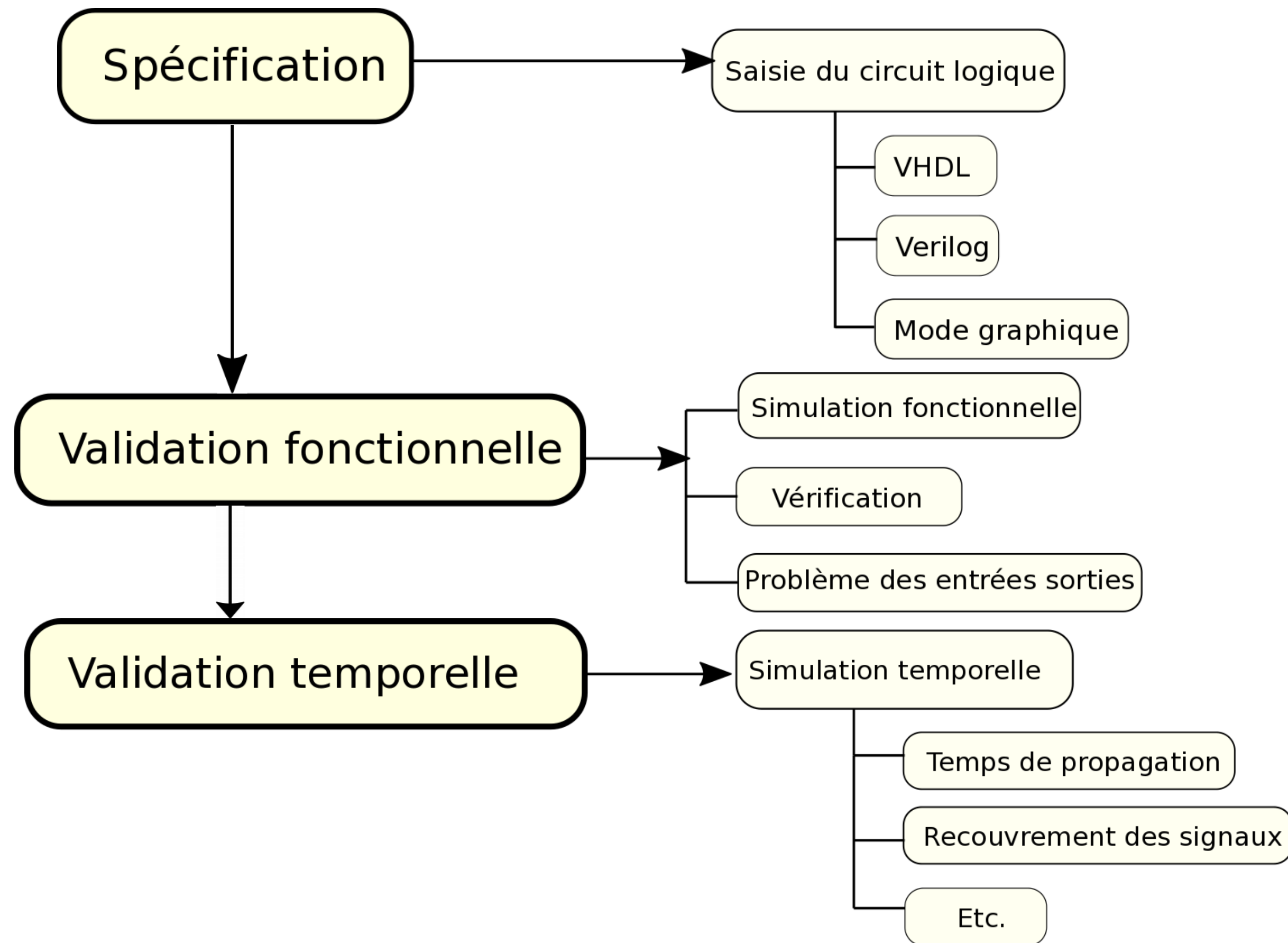
Méthodologie de conception des FPGA (CPLD)



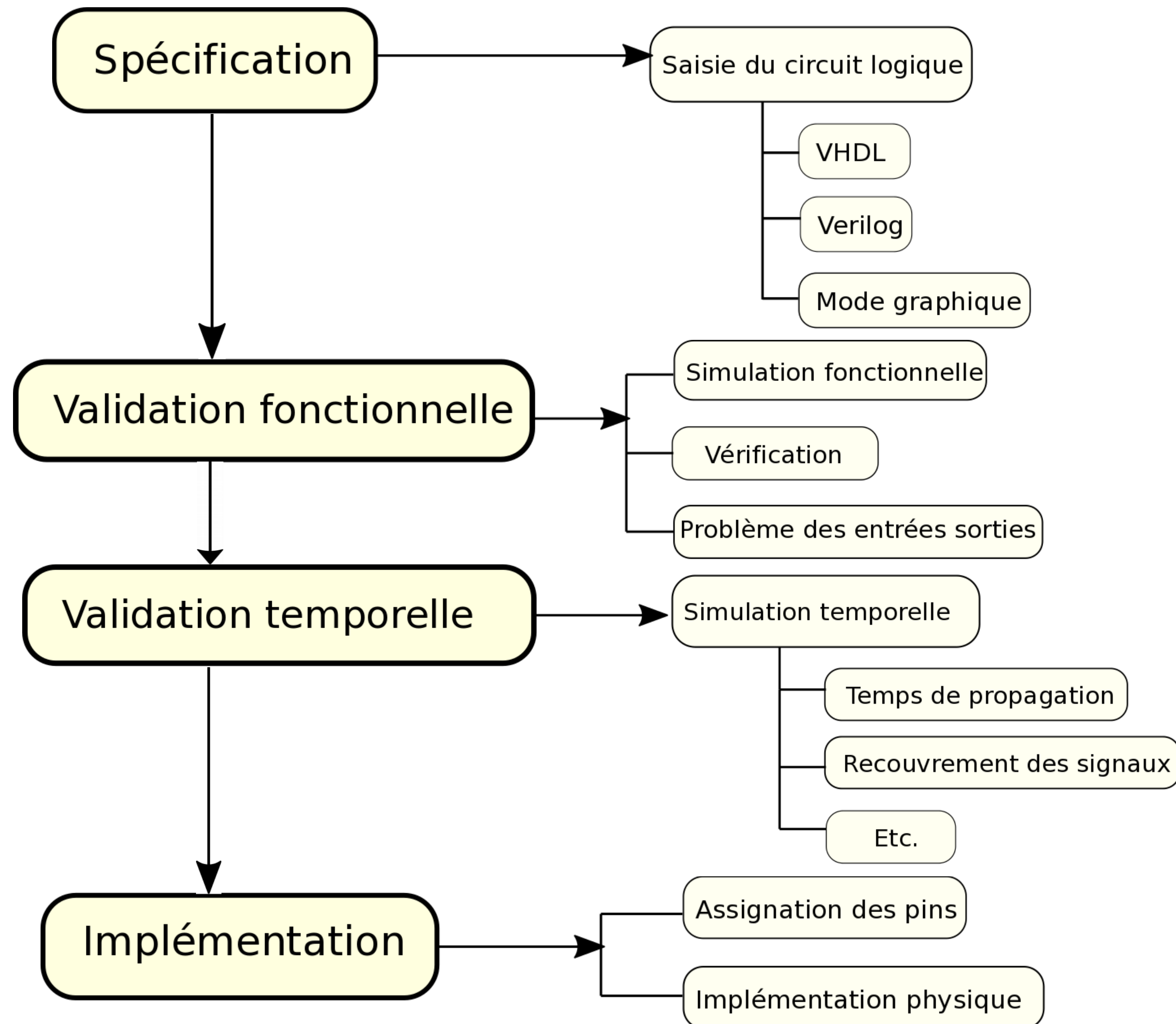
Méthodologie de conception des FPGA (CPLD)



Méthodologie de conception des FPGA (CPLD)



Méthodologie de conception des FPGA (CPLD)



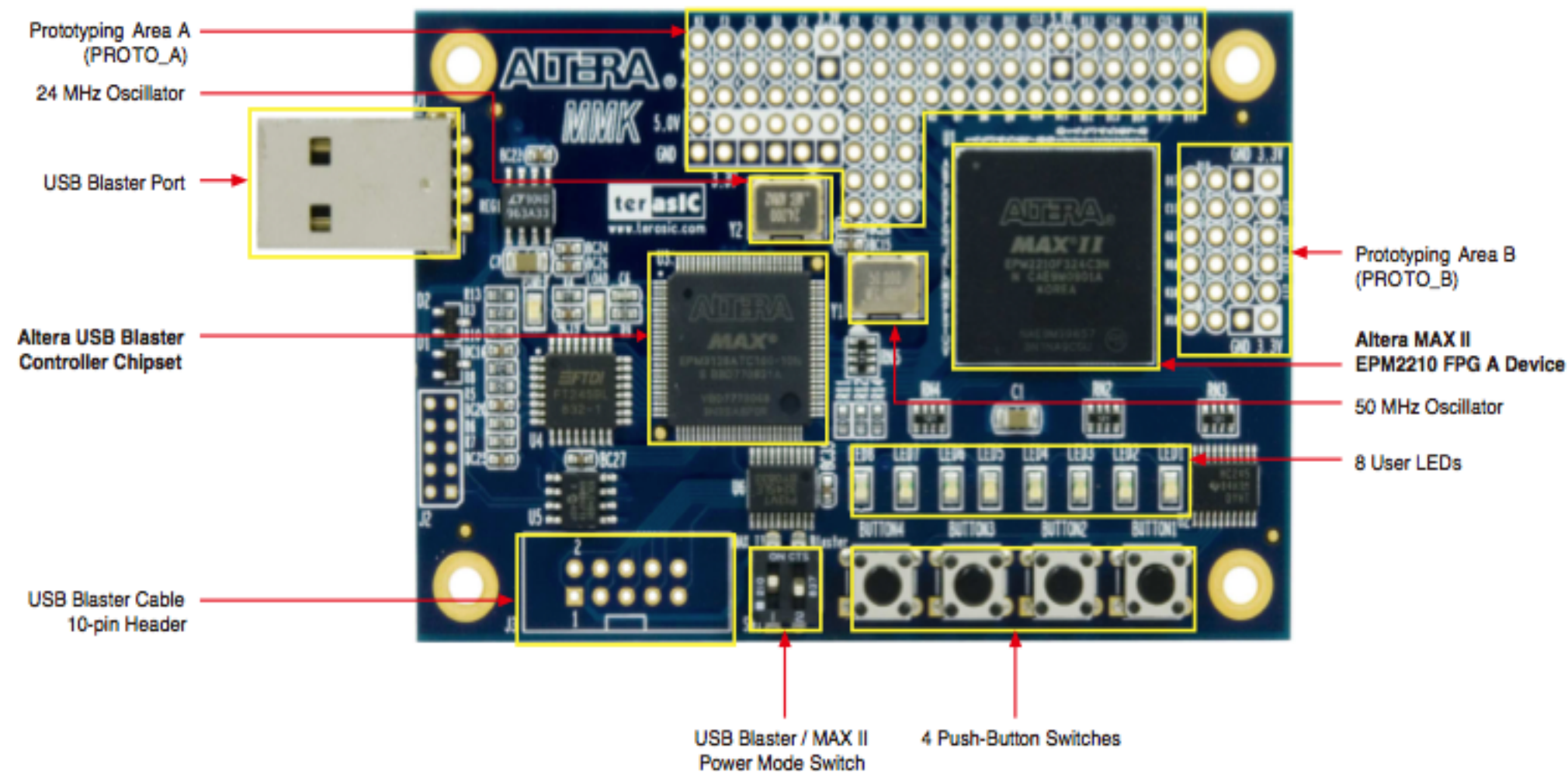
- Synthèse avec les deux principales plateformes de développement

- Altera Quartus II
- Xilinx ISE

- Simulation.

- ModelSim

CARTE DEO (NANO) (ALTERA)



Specifications FPGA

- Altera MAX II EPM2210F324 FPGA device

I/O Devices

- Built-in USB Blaster for FPGA configuration

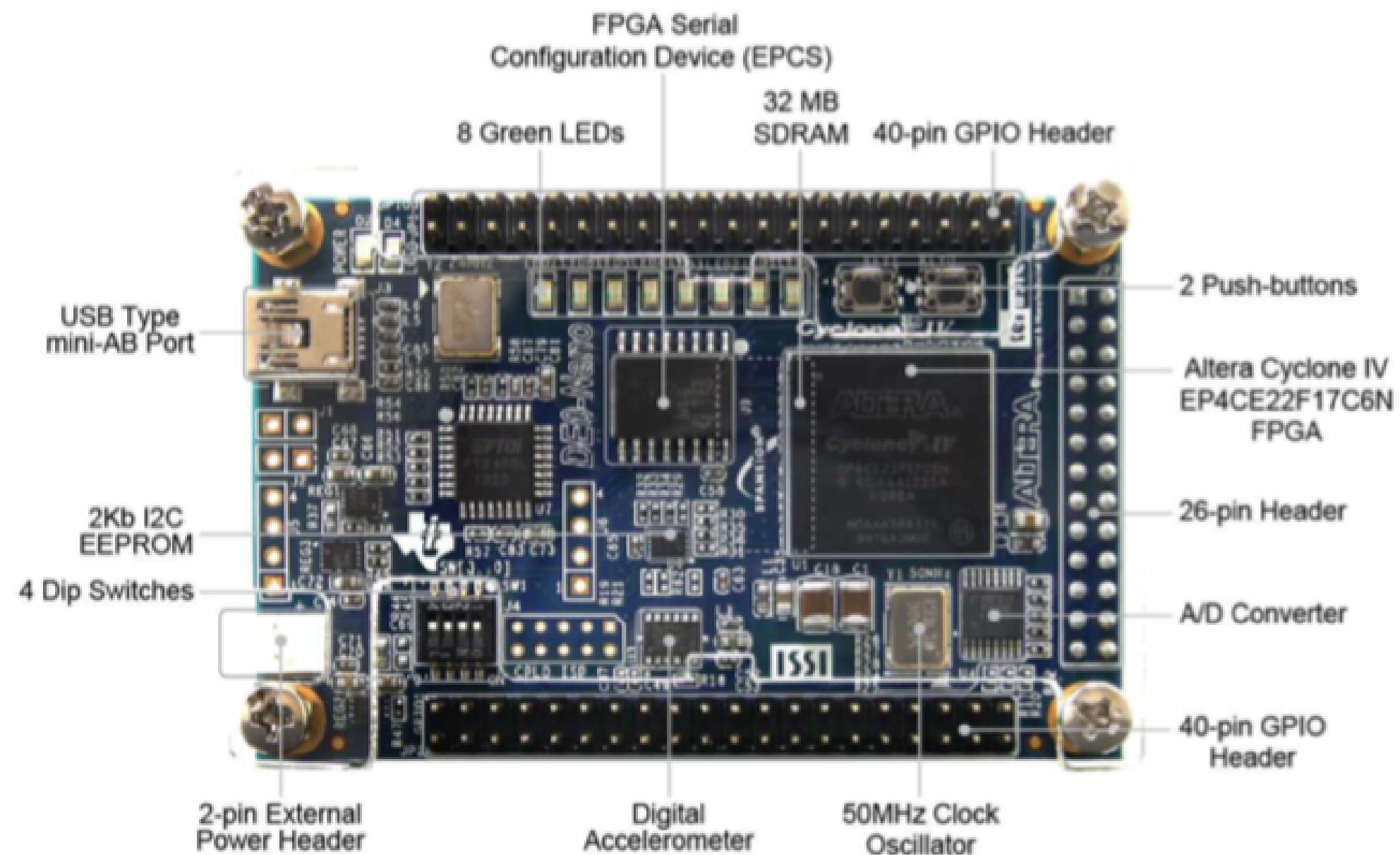
Switches, LEDs, and Clocks

- 1 DIP switch
- 4 pushbutton switches
- 2 red user LEDs,
- 2 yellow user LEDs,
- 2 blue user LEDs,
- 2 green user LEDs
- 50-MHz oscillator for clock sources
- Powered by USB

Prototyping Areas

- A 40-pin expansion port area compatible with Altera DE2/DE1 expansion ports.
- Prototyping Area A with **68 GPIO**, **6 3.3V**, **2 5V** and **8 GND** pins
- Prototyping Area B with **20 GPIO**, **2 3.3V**, and **2 GND** pins

CARTE DEO (NANO) (ALTERA)



Specifications FPGA

- Altera CYCLONE IV EP4CE22F17C6N FPGA device
- 256 pins, 47 cellules

I/O Devices

- Built-in USB Blaster for FPGA configuration

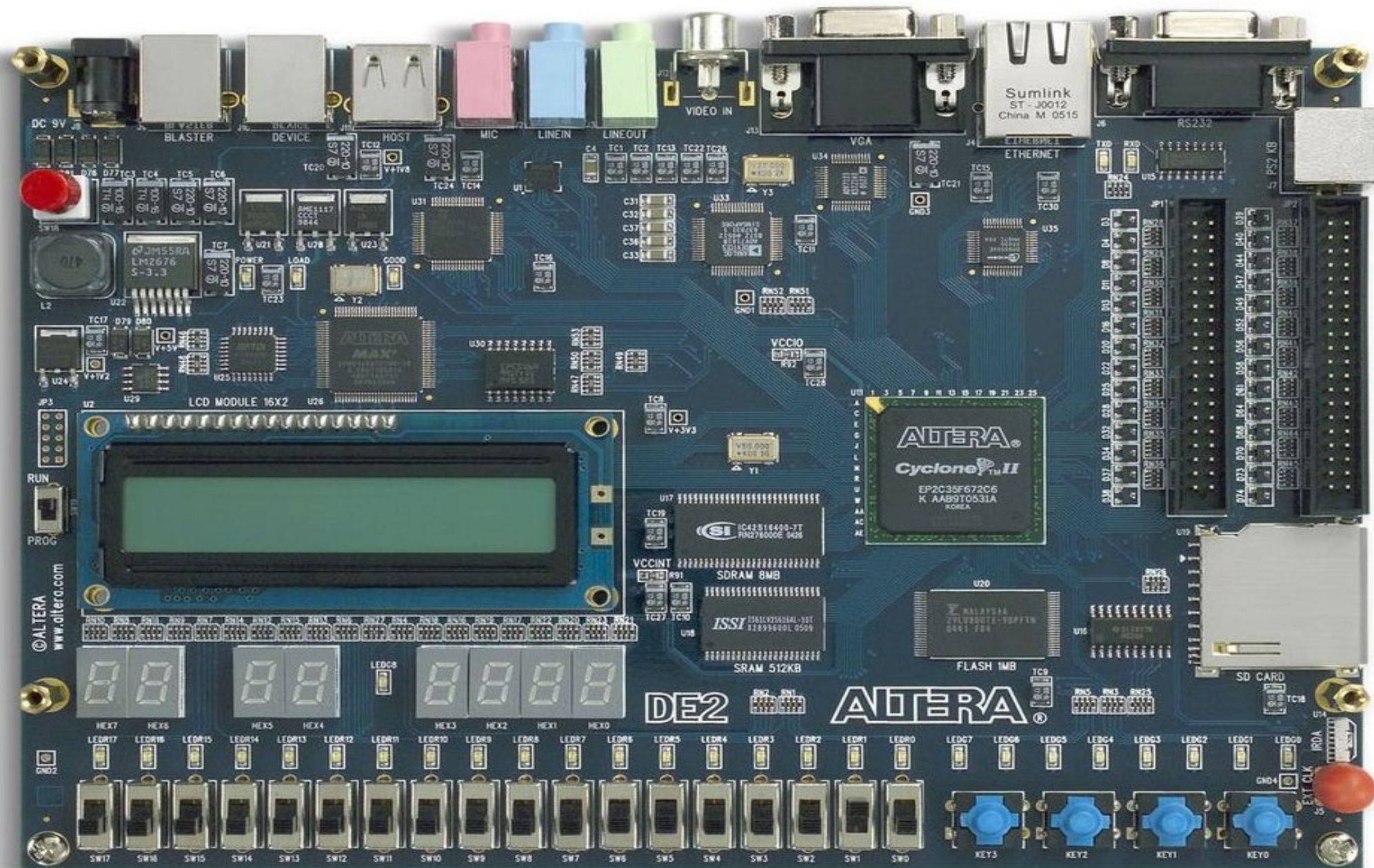
Switches, LEDs, Displays, and Clocks

- 4 DIP switch
- 2 pushbutton switches
- 2 red user LEDs,
- 2 yellow user LEDs,
- 2 blue user LEDs,
- 2 green user LEDs
- 50-MHz oscillator for clock sources
- Powered by USB
- . A/D Converter, 8 channel – 12 bit A/D Converter

Prototyping Areas

- Two 40-pin Headers GPIO compatible provide 72 I/O pin, 5V Power pin, Two 3,3V and four ground pins .
- 32MB SDRAM, 2Kb I2C EEPROM

CARTE DE2 (ALTERA)



Specifications FPGA

- Cyclone II EP2C35F672C6 FPGA
- 672 pins, 4276 cellules

I/O Devices

- Built-in USB Blaster for FPGA configuration
- 10/100 Ethernet, RS-232, Infrared port
- Video Out (VGA 10-bit DAC)
- Video In (NTSC/PAL/Multi-format)
- USB 2.0 (type A and type B)
- PS/2 mouse or keyboard port
- Line-in, Line-out, microphone-in (24-bit audio CODEC)
- Expansion headers (76 signal pins)

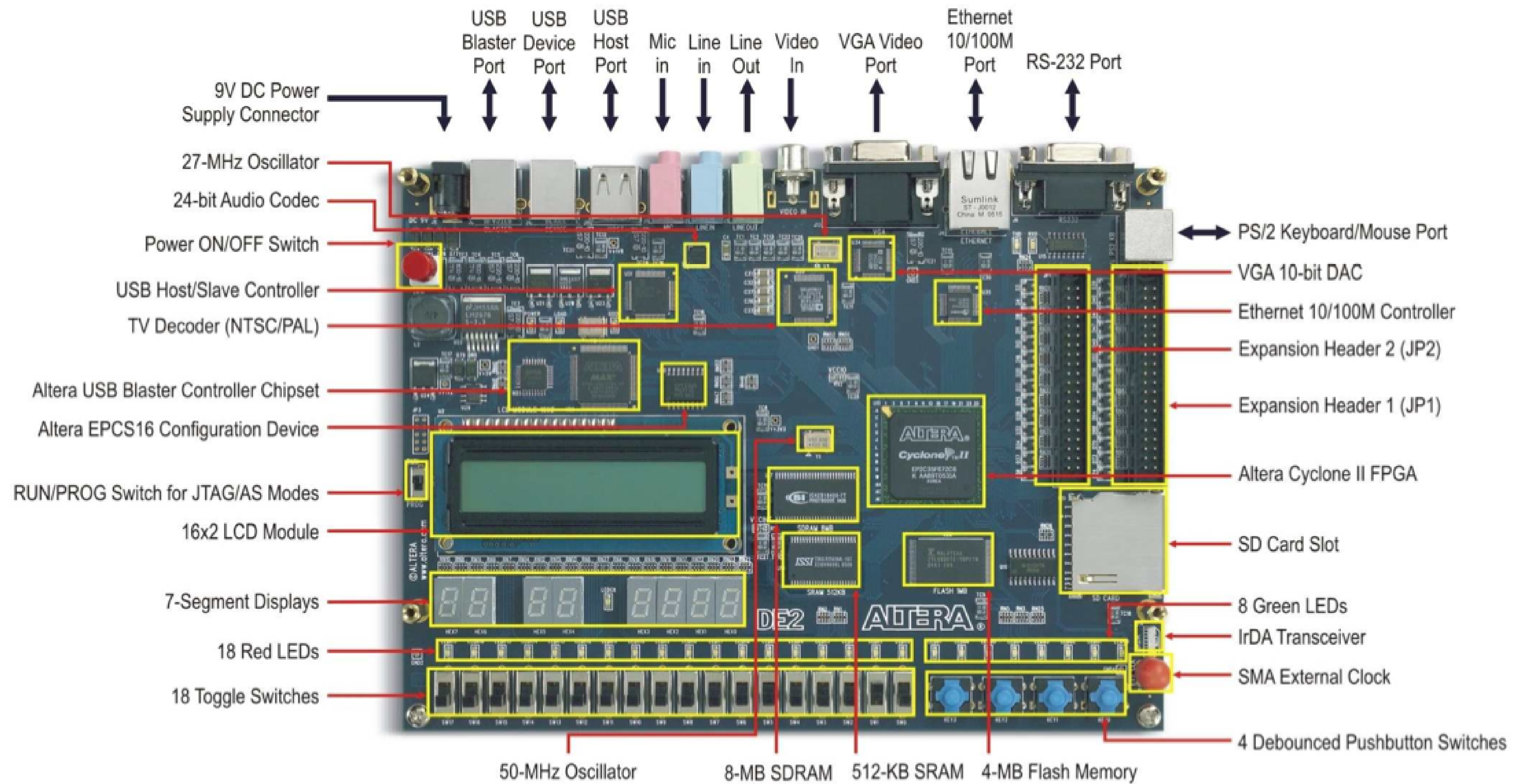
Memory

- 8-MB SDRAM, 512-KB SRAM, 4-MB Flash
- SD memory card slot

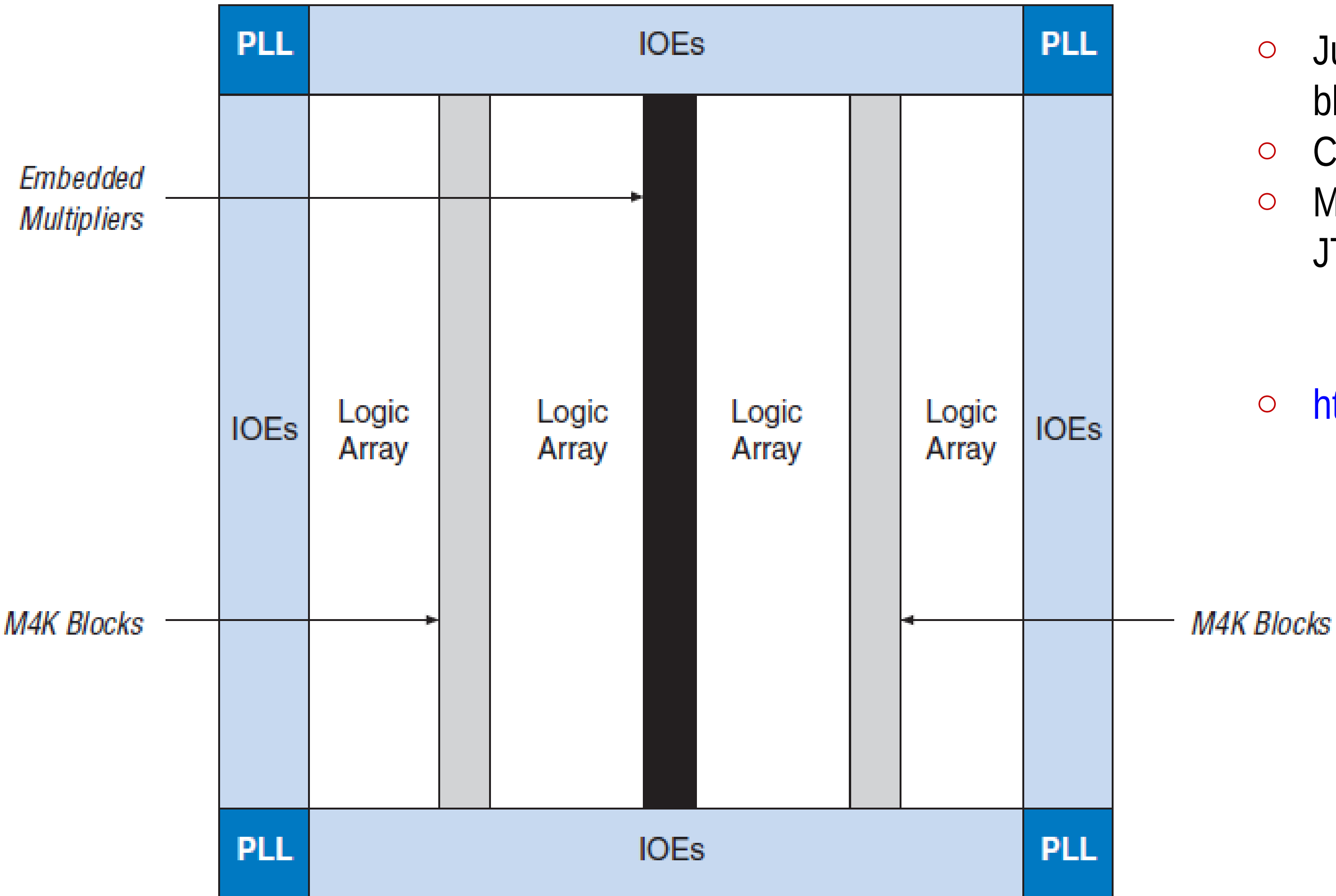
Switches, LEDs, Displays, and Clocks

- 18 toggle switches
- 4 debounced pushbutton switches
- 18 red LEDs, 8 green LEDs
- Eight 7-segment displays
- 16 x 2 LCD display
- 27-MHz and 50-MHz oscillators, external SMA clock input

CARTE DE2 (ALTERA)

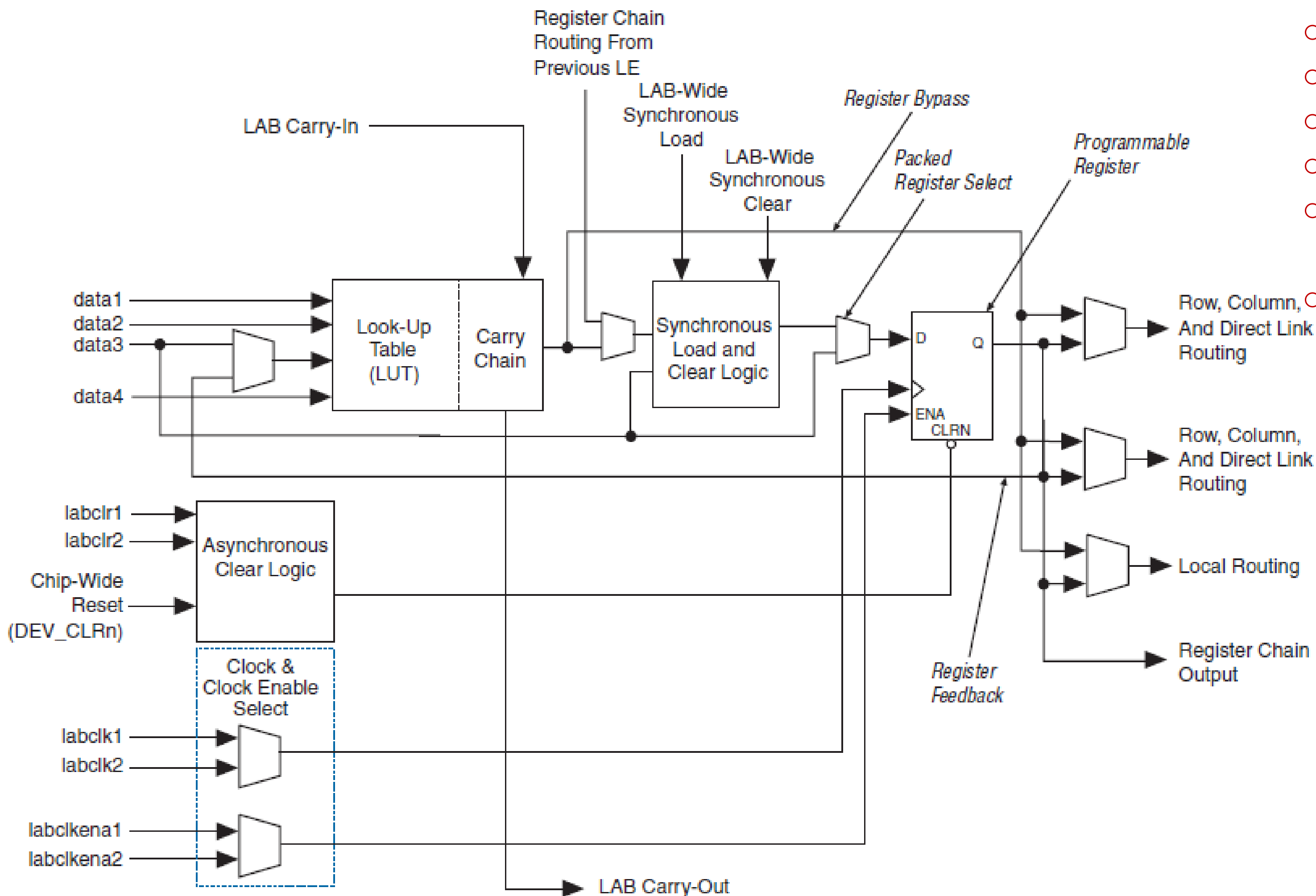
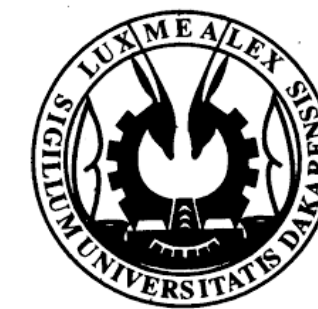


Exemple d'ALTERA : Le cyclone II



- Jusqu'à 68416 éléments logiques regroupés par blocs de 16
- Configuration rapide en moins de 100ms
- Mode de configuration série USB BLASTER ou JTAG
- <https://www.altera.com>

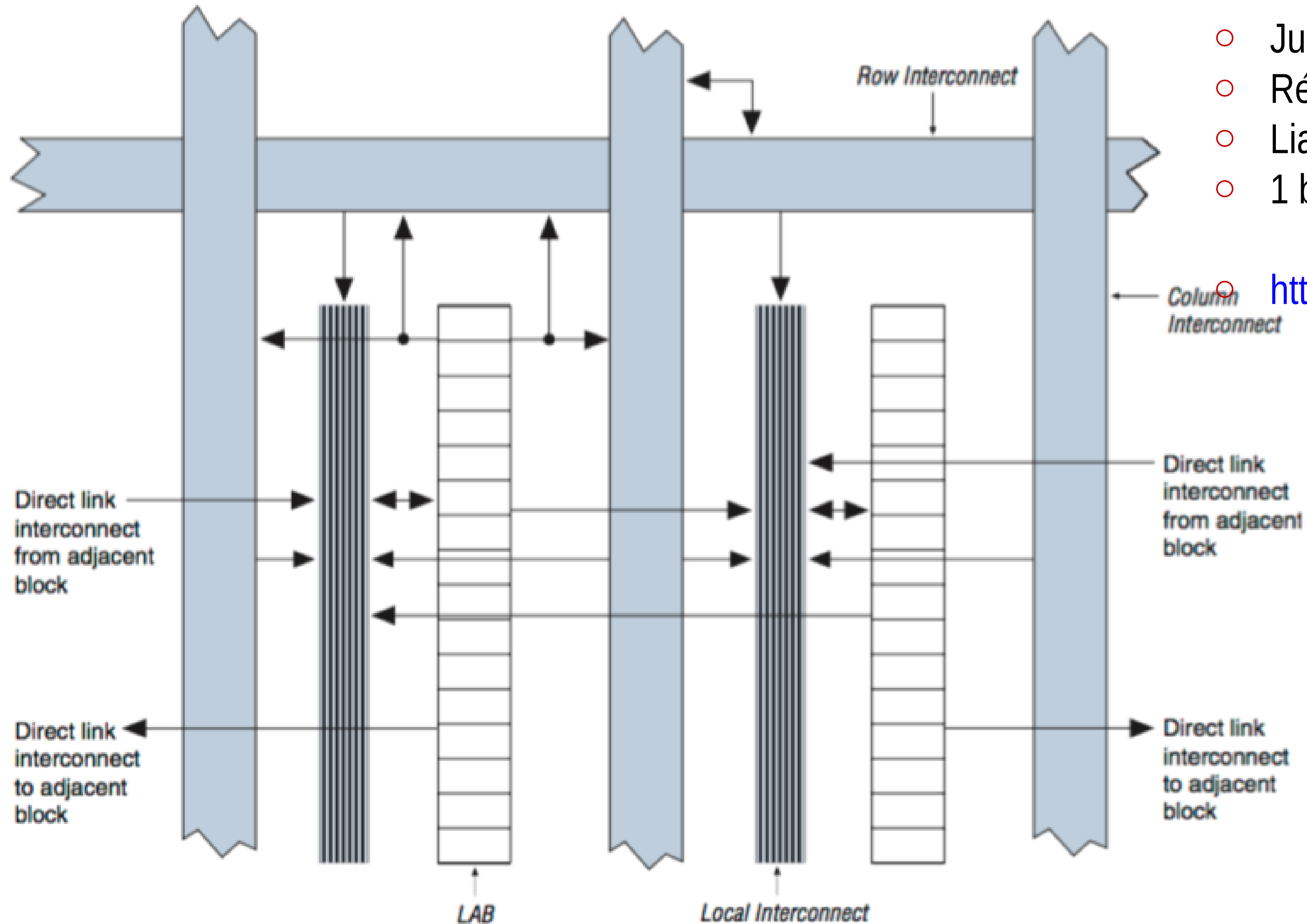
Cyclone II (architecture d'un élément logique)



- 4 entrées
- 1 registre de sortie programmable
- 1 entrée de retenue
- 1 sortie de retenue
- Interconnexion local

<https://www.altera.com>

Cyclone II (interconnexions des blocs logiques)



- Jusqu'à 68416 éléments logiques
- Réseau local d'interconnexion
- Liaisons directes avec BL adjacent
- 1 bloc mémoire, Ck, I/O entre BL adjacent

○ <https://www.altera.com>

● QUARTUS II Web Edition

- Logiciel permettant le développement jusqu'à l'implémentation sur la carte FPGA
- Téléchargement gratuit sur www.altera.com

● Simulateur ModelSim-Altera Web Edition.

● Carte de développement DE0 et DE2

Prise en main de Quartus II



The screenshot displays the Quartus II 32-bit software interface. The main window is titled "Getting Started With Quartus II Software" and features the following elements:

- Start Designing:** Includes buttons for "Create a New Project (New Project Wizard)" and "Open Existing Project".
- Start Learning:** Includes a button for "Open Interactive Tutorial".
- Open Recent Project:** Lists recent projects with their file paths:
 - C:/Documents/Altera_Project/Compteur_10/Compteur_10.qpf
 - C:/Documents/Altera_Project/Test1/test1.qpf
 - C:/Documents/Altera_Project/XOR/Ouexclusif.qpf
 - C:/Documents/Altera/XOR/Ouexclusif.qpf
- Navigation Links:** "Web vs. Subscription Edition", "Buy Subscription", "Literature", "Training", "Online Demos", and "Support".
- Footer:** "ALTERA" logo and a checkbox "Don't show this screen again".

On the left side of the interface, the "Project Navigator" pane shows a "Compilation Hierarchy" tree. Below it, the "Tasks" pane is set to "Flow: Compilation" and lists tasks such as "Compile Design", "Analysis & Synthesis", "Fitter (Place & Route)", "Assembler (Generate programming files)", "TimeQuest Timing Analysis", "EDA Netlist Writer", and "Program Device (Open Programmer)".

At the bottom, the "Messages" pane is visible, showing a search bar and tabs for "System", "Processing", "Extra Info", "Info", "Warning", "Critical Warning", "Error", "Suppressed", and "Flag". The Windows taskbar at the very bottom shows the time as 09:24 on 09/02/2016.

Prise en main de Quartus II



Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

Primed to Perform
Go faster on next generation devices with the Spectra-Q™ engine.
Introducing the New Software ▶ **Quartus Prime** Design Software

ALTERA
QUARTUS II
Version 12.0

Task
▶ Compile Design
▶ Analysis & Synthesis
▶ Fitter (Place & Route)
▶ Assembler (Generate programming files)
▶ TimeQuest Timing Analysis
▶ EDA Netlist Writer
▶ Program Device (Open Programmer)

Buy Software
Download New Software Release
Documentation

Starts the New Project Wizard
0% 00:00:00

09:25
09/02/2016

Prise en main de Quartus II



Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Primed to Perform

Go faster on next generation devices with the Spectra-Q™ engine.

Introducing the New Software

Quartus Prime Design Software

New Project Wizard

Introduction

The New Project Wizard helps you create a new project and preliminary project settings, including the following:

- Project name and directory
- Name of the top-level design entity
- Project files and libraries
- Target device family and device
- EDA tool settings

You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.

Don't show me this introduction again

< Back Next > Finish Cancel Help

Buy Software

Download New Software Release

Documentation

Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Location: 0% 00:00:00

09:25 09/02/2016

Prise en main de Quartus II



The screenshot displays the Quartus II 32-bit software interface. The main window is titled "Quartus II 32-bit" and features a menu bar (File, Edit, View, Project, Assignments, Processing, Tools, Window, Help) and a toolbar. A "Project Navigator" pane on the left shows a "Compilation Hierarchy" tree. The central workspace contains a "Primed to Perform" banner for Quartus Prime Design Software. A "New Project Wizard" dialog box is open, titled "New Project Wizard" and "Directory, Name, Top-Level Entity [page 1 of 5]". The wizard prompts for the working directory (C:/Documents/Altera_Project/compteur_fpga), project name (compteur_10), and top-level design entity name (compteur_10). A "Use Existing Project Settings..." button is also present. The wizard has navigation buttons: < Back, Next >, Finish, Cancel, and Help. In the bottom right corner of the main window, there are buttons for "Buy Software", "Download New Software Release", and "Documentation". The bottom of the screen shows a Windows taskbar with icons for Internet Explorer, File Explorer, Google Chrome, PowerPoint, and a globe icon. The system tray displays the time as 09:26 on 09/02/2016.

Prise en main de Quartus II



Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

New Project Wizard

Add Files [page 2 of 5]

Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.

File name: ...

File Name	Type	Library	Design Entry/Synthesis Tool	HDL Version
-----------	------	---------	-----------------------------	-------------

Specify the path names of any non-default libraries.

< Back Next > Finish Cancel Help

Messages

Type Message

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

Location: Locate

0% 00:00:00

09:27 09/02/2016

Prise en main de Quartus II



Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Primed to Perform
Go faster on next generation devices with the Spectra-Q™ engine.
Introducing the New Software ▶ **Quartus Prime** Design Software

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family
Family: Cyclone IV E
Devices: All

Target device
 Auto device selected by the Fitter
 Specific device selected in 'Available devices' list
 Other: n/a

Show in 'Available devices' list
Package: FBGA
Pin count: 256
Speed grade: 6
Name filter:
 Show advanced devices HardCopy compatible only

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	jal Clo
EP4CE6F17C6	1.2V	6272	180	276480	30	2	10
EP4CE10F17C6	1.2V	10320	180	423936	46	2	10
EP4CE15F17C6	1.2V	15408	166	516096	112	4	20
EP4CE22F17C6	1.2V	22320	154	608256	132	4	20

Companion device
HardCopy:
 Limit DSP & RAM to HardCopy device resources

< Back Next > Finish Cancel Help

Buy Software
Download New Software Release
Documentation

Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

0% 00:00:00

09:27 09/02/2016

Prise en main de Quartus II



The screenshot shows the Quartus II 32-bit software interface. The main window displays a 'Primed to Perform' banner for Quartus Prime Design Software. A 'New Project Wizard' dialog box is open, showing the 'EDA Tool Settings [page 4 of 5]' screen. The dialog box prompts the user to specify other EDA tools used with the Quartus II software. The 'EDA tools' section contains a table with the following data:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synthesis	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	ModelSim-Altera	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Formal Verification	<None>		
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

The dialog box also features navigation buttons: '< Back', 'Next >', 'Finish', 'Cancel', and 'Help'. In the bottom right corner of the dialog, there are three buttons: 'Buy Software', 'Download New Software Release', and 'Documentation'. The background interface includes a 'Project Navigator' on the left, a 'Tasks' pane, and a 'Messages' pane at the bottom. The Windows taskbar at the very bottom shows the time as 09:27 on 09/02/2016.

Prise en main de Quartus II



Quartus II 32-bit

File Edit View Project Assignments Processing Tools Window Help

Search altera.com

Project Navigator

Compilation Hierarchy

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

Project directory:	C:/Documents/Altera_Project/compteur_fpga
Project name:	compteur_10
Top-level design entity:	compteur_10
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	Cyclone IV E
Device:	EP4CE22F17C6
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	ModelSim-Altera (VHDL)
Timing analysis:	0
Operating conditions:	
VCCINT voltage:	1.2V
Junction temperature range:	0-85 °C

< Back Next > Finish Cancel Help

Buy Software

Download New Software Release

Documentation

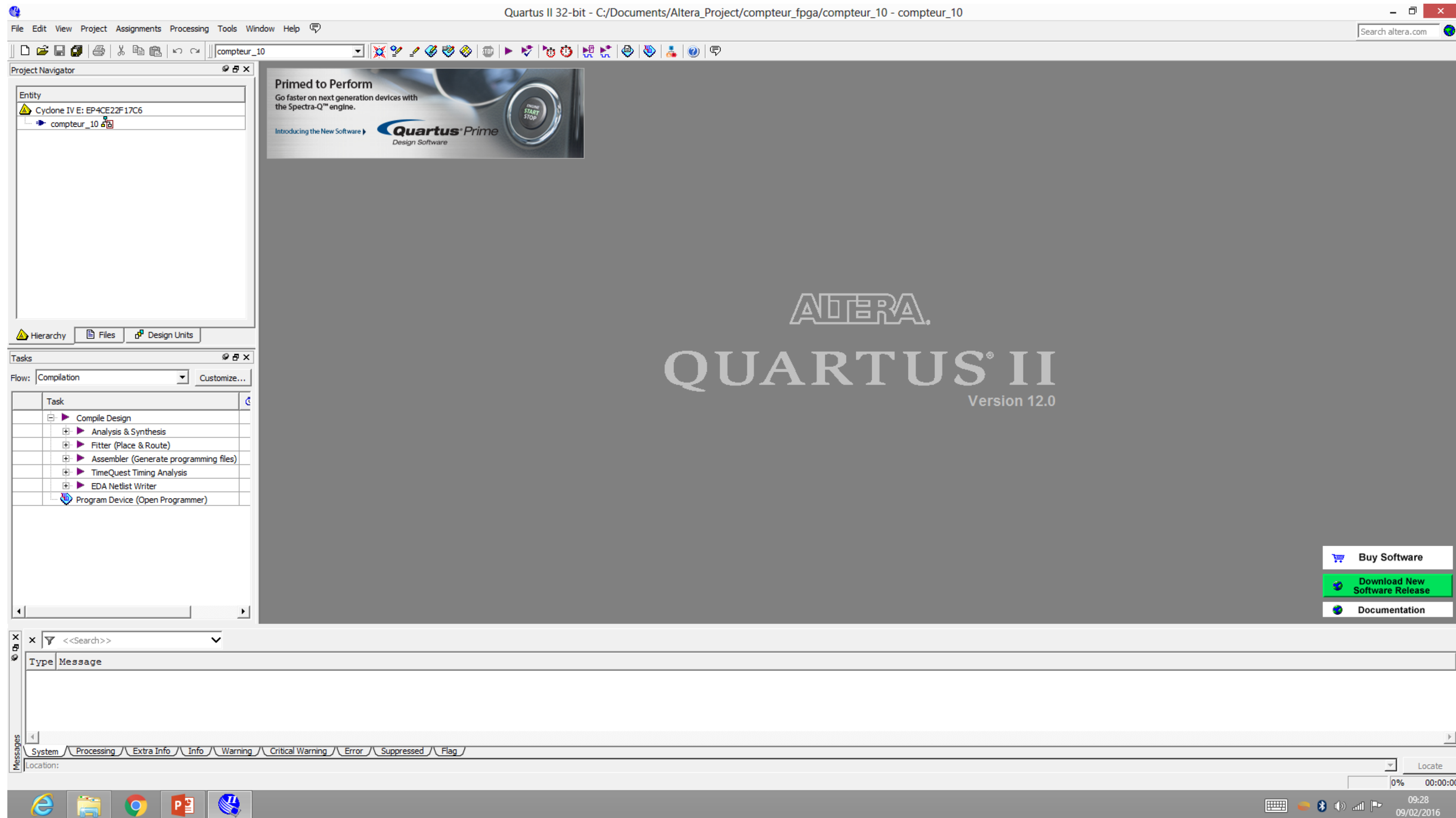
Messages

System Processing Extra Info Info Warning Critical Warning Error Suppressed Flag

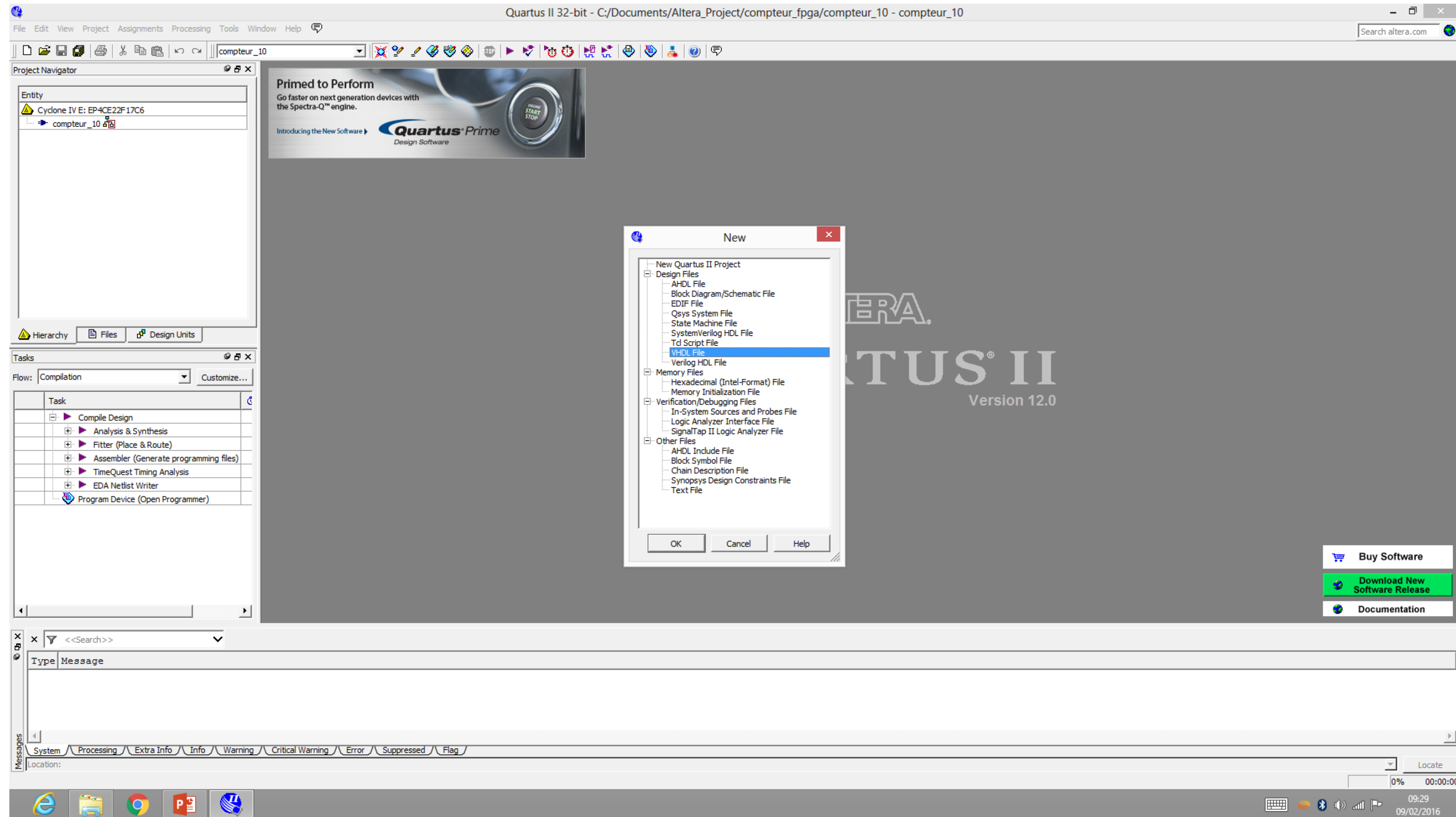
Location: 0% 00:00:00

09:28 09/02/2016

Prise en main de Quartus II



Prise en main de Quartus II



Prise en main de Quartus II



The screenshot displays the Quartus II software interface. The main window shows the VHDL code for a counter named 'Compteur_10'. The code includes library declarations, entity and architecture definitions, and a process block for counting. The Project Navigator on the left shows the project structure, and the Tasks window below it lists various design tasks. The Messages window at the bottom is currently empty.

```
1  Library ieee;
2  Use ieee.std_logic_1164.all;
3  Use ieee.numeric_std.all;
4
5  ENTITY Compteur_10 IS
6  PORT (Ck, R : IN STD_LOGIC;
7        Q: OUT  STD_LOGIC_VECTOR (3 downto 0));
8  END Compteur_10;
9
10 ARCHITECTURE Structural OF Compteur_10 IS
11   SIGNAL Qa: STD_LOGIC_VECTOR (3 downto 0);
12 BEGIN
13   PROCESS (Ck, R)  -- liste de sensibilit
14   BEGIN
15     IF R = '0' then
16       Qa <= "0000";
17     ELSIF Ck'event and Ck = '1' then  -- validation du front montant
18       Qa <= STD_LOGIC_VECTOR(UNSIGNED (Qa) + 1);
19       IF Qa="1010" THEN Qa <= "0000";
20     END IF;
21   END IF;
22 END PROCESS;
23   Q <= Qa;
24
25 END Structural;
26
```

Prise en main de Quartus II



The screenshot displays the Quartus II 32-bit IDE. The main window shows a VHDL file named 'Compteur_10.vhd' with the following code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity Compteur_10 is
    port (
        R : IN STD_LOGIC;
        Ck : IN STD_LOGIC_VECTOR (3 downto 0));
end Compteur_10;

architecture Structural of Compteur_10 is
    signal Qa : STD_LOGIC_VECTOR (3 downto 0);
begin
    process (Ck, R) -- liste de sensibilit 
    begin
        if R = '0' then
            Qa <= "0000";
        elsif Ck'event and Ck = '1' then -- validation du front montant
            Qa <= STD_LOGIC_VECTOR(unsigned(Qa) + 1);
            if Qa="1010" THEN Qa <= "0000";
            end if;
        end if;
    end process;
    Q <= Qa;
end Structural;
```

The left sidebar shows the Project Navigator with the entity 'Compteur_10' selected. The 'Tasks' window is open, showing a list of compilation tasks:

Task
Compile Design
Analysis & Synthesis
Fitter (Place & Route)
Assembler (Generate programming files)
TimeQuest Timing Analysis
EDA Netlist Writer
Program Device (Open Programmer)

The bottom status bar indicates 'Starts a new compilation' with a progress indicator at 0% and a timer at 00:00:00. The Windows taskbar at the bottom shows the system tray with the date 09/02/2016 and time 09:31.

Prise en main de Quartus II



Quartus II 32-bit - C:/Documents/Altera_Project/compteur_fpga/compteur_10 - compteur_10

File Edit View Project Assignments Processing Tools Window Help

compteur_10

Project Navigator

Entity

- Cyclone IV E: EP4CE22F17C6
- Compteur_10

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	Time
Compile Design	00
Analysis & Synthesis	00
Fitter (Place & Route)	00
Assembler (Generate programming files)	00
TimeQuest Timing Analysis	00
EDA Netlist Writer	00
Program Device (Open Programmer)	

Flow Summary

Flow Status: Successful - Tue Feb 09 09:32:30 2016

Quartus II 32-bit Version: 12.0 Build 263 08/02/2012 SP 2 SJ Web Edition

Revision Name: compteur_10

Top-level Entity Name: Compteur_10

Family: Cyclone IV E

Device: EP4CE22F17C6

Timing Models: Final

Total logic elements: 4 / 22,320 (< 1 %)

- Total combinational functions: 4 / 22,320 (< 1 %)
- Dedicated logic registers: 4 / 22,320 (< 1 %)

Total registers: 4

Total pins: 6 / 154 (4 %)

Total virtual pins: 0

Total memory bits: 0 / 608,256 (0 %)

Embedded Multiplier 9-bit elements: 0 / 132 (0 %)

Total PLLs: 0 / 4 (0 %)

Quartus II

Full Compilation was successful (11 warnings)

OK

Messages

Type Message

- Info (204019): Generated file compteur_10_min_1200mv_0c_vhd_fast.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
- Info (204019): Generated file compteur_10_vhd.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
- Info: Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
- Info (293026): Skipped module PowerPlay Power Analyzer due to the assignment FLOW_ENABLE_POWER_ANALYZER
- Info (293000): Quartus II Full Compilation was successful. 0 errors, 11 warnings

System Processing (112) Extra Info Info (101) Warning (5) Critical Warning (6) Error Suppressed (6) Flag

Location: 100% 00:00:16

09:32 09/02/2016

Prise en main de Quartus II



● Validation du circuit

Prise en main de Quartus II



The screenshot displays the Quartus II 32-bit software interface. The main window shows a compilation report for a project named 'compteur_10'. The report indicates a successful compilation on Tuesday, February 9, 2016, at 09:32:30. The report details the version (12.0 Build 263 08/02/2012 SP 2 SJ Web Edition) and the target device (Cyclone IV E EP4CE22F17C6). The report also lists resource usage statistics, such as the number of logic elements, flip-flops, and registers used.

The left sidebar shows the Project Navigator with the entity 'Compteur_10' selected. The Tools menu is open, showing various simulation and analysis tools. The Messages window at the bottom displays the following log entries:

```
Info (204019): Generated file compteur_10_min_1200mv_0c_vhd_fast.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
Info (204019): Generated file compteur_10_vhd.sdo in folder "C:/Documents/Altera_Project/compteur_fpga/simulation/modelsim/" for EDA simulation tool
Info: Quartus II 32-bit EDA Netlist Writer was successful. 0 errors, 0 warnings
Info (293026): Skipped module PowerPlay Power Analyzer due to the assignment FLOW_ENABLE_POWER_ANALYZER
Info (293000): Quartus II Full Compilation was successful. 0 errors, 11 warnings
```

The bottom status bar shows the current task: 'Runs the specified RTL simulation tool'.

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Process Tools Layout Bookmarks Window Help

ColumnLayout AllColumns

Library

Name	Type	Path
work	Library	rtl_work
rtl_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH/./altera/vhd/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhd/altera
altera_Insim	Library	\$MODEL_TECH/./altera/vhd/altera_...
altera_Insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH/./altera/vhd/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhd/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhd/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhd/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhd/arriagx_...
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhd/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhd/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhd/arriaii_p...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhd/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhd/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhd/arriaiigz...

Objects

Name	Value	Kind	Mode
------	-------	------	------

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
------	-----------------	-------	-------	-------------

Transcript

```
# -- Compiling architecture Structural of Compteur_10
#
ModelSim>
```

<No Design Loaded> <No Context>

Messages

Type	Message
Info (22036)	Successfully launched NativeLink simulation (quartus_sh -t "c:/altera/12.0sp2/quartus/common/tcl/internal/nativelink/qnativesim.tcl" --rtl_sim "compteur_10" "compteur_10")
Info (22036)	For messages from NativeLink execution see the NativeLink log file C:/Documents/Altera_Project/compteur_fpga/compteur_10_nativelink_simulation.rpt

System (2) Processing (112) Extra Info Info (101) Warning (5) Critical Warning (6) Error Suppressed (6) Flag

Location: 100% 00:00:16

09:34 09/02/2016

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_work
comp	Library	Project/compte...
rt_work	Library	Project/compte...
220mod	Library	tera/vhdl/220model
220mod	Library	tera/verilog/220m...
altera	Library	tera/vhdl/altera
altera_in	Library	tera/vhdl/altera_...
altera_in	Library	tera/verilog/altera...
altera_m	Library	tera/vhdl/altera_mf
altera_m	Library	tera/verilog/altera...
altera_v	Library	tera/verilog/altera
altgxb	Library	tera/vhdl/altgxb
altgxb_i	Library	tera/vhdl/altgxb
altgxb_v	Library	tera/verilog/altgxb
arriagx	Library	tera/vhdl/arriagx
arriagx	Library	tera/vhdl/arriagx...
arriagx	Library	tera/verilog/arriag...
arriagx	Library	tera/verilog/arriagx
arriai	Library	tera/vhdl/arriai
arriai_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriai_hssi
arriai_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriai_p...
arriai_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_ver	Library	\$MODEL_TECH/./altera/verilog/arriai
arriai_gz	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz
arriai_gz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz...
arriai_gz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_gz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz...
arriai_gz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_gz_ver	Library	\$MODEL_TECH/./altera/verilog/arriai_gz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...)	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone
cydoneii	Library	\$MODEL_TECH/./altera/vhdl/cydoneii
cydoneii_ver	Library	\$MODEL_TECH/./altera/verilog/cydoneii
cydoneiii	Library	\$MODEL_TECH/./altera/vhdl/cydoneiii
cydoneiii_ver	Library	\$MODEL_TECH/./altera/verilog/cydo...

Objects

Name	Value	Kind	Mode
------	-------	------	------

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
------	-----------------	-------	-------	-------------

Transcript

```
# -- Compiling architecture Structural of Compteur_10
#
ModelSim>
```

<No Design Loaded> compteur_10

09:34 09/02/2016

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_work
comp_teur_10	Library	Project/compte...
rt_work	Library	Project/compte...
220mod	Library	tera/vhdl/220model
220mod	Library	tera/verilog/220m...
altera	Library	tera/vhdl/altera
altera_l	Library	tera/vhdl/altera_l...
altera_l	Library	tera/verilog/altera...
altera_n	Library	tera/vhdl/altera_mf
altera_n	Library	tera/verilog/altera...
altera_v	Library	tera/verilog/altera
altgxb	Library	tera/vhdl/altgxb
altgxb_l	Library	tera/vhdl/altgxb
altgxb_	Library	tera/verilog/altgxb
arriagx	Library	tera/vhdl/arriagx
arriagx_	Library	tera/vhdl/arriagx_...
arriagx_	Library	tera/verilog/arriag...
arriagx_	Library	tera/verilog/arriagx
arriai	Library	tera/vhdl/arriai
arriai_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriai_hssi
arriai_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriai_p...
arriai_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_ver	Library	\$MODEL_TECH/./altera/verilog/arriai
arriai_gz	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz
arriai_gz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz...
arriai_gz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_gz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriai_gz...
arriai_gz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriai...
arriai_gz_ver	Library	\$MODEL_TECH/./altera/verilog/arriai_gz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...)	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone
cydoneii	Library	\$MODEL_TECH/./altera/vhdl/cydoneii
cydoneii_ver	Library	\$MODEL_TECH/./altera/verilog/cydoneii
cydoneii	Library	\$MODEL_TECH/./altera/vhdl/cydoneii

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
line__23	VHDL Process	Active	1	/compteur_10
line__13	VHDL Process	Ready	2	/compteur_10

Transcript

```
# Loading ieee.numeric_std(body)
# Loading work.compteur_10(structural)
VSIM 3>
```

Now: 0 ps Delta: 0 sim:/compteur_10

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Library Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_work
compteur_10	Entity	C:/Documents/Altera_Project/compte...
rt_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_insim	Library	\$MODEL_TECH/./altera/vhdl/altera_1...
altera_insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriagx...
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_p...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...)	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
line__23	VHDL Process	Active	1	/compteur_10
line__13	VHDL Process	Ready	2	/compteur_10

Wave - Default

Msgs
Edit:/compteur_10/Ck No Data
Edit:/compteur_10/R No Data
Edit:/compteur_10/Q No Data

Transcript

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10
V$IM 6>
```

Now: 0 ps Delta: 0 sim:/compteur_10

09:35 09/02/2016

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_work
compteur_10	Entity	C:/Documents/Altera_Project/compte...
rt_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_insim	Library	\$MODEL_TECH/./altera/vhdl/altera_...
altera_insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriagx...
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_p...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Processes (Active)

Name	Type (filtered)	State	Order	Parent Path
line__23	VHDL Process	Active	1	/compteur_10
line__13	VHDL Process	Ready	2	/compteur_10

Wave - Default

Msgs

Now 0 ps

Cursor 1 0 ps

0 ps to 1 ns

Transcript

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10
VSIM 6>
```

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_l_work
compteur_10	Entity	C:/Documents/Altera_Project/compte...
rt_l_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_insim	Library	\$MODEL_TECH/./altera/vhdl/altera_...
altera_insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriagx...
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_p...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...)	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Wave - Default

Signal	Value
Edit:/compteur_10/Ck	No Data
Edit:/compteur_10/R	No Data
Edit:/compteur_10/Q	No Data

Create Pattern Wizard

Generate a waveform for any signal for the chosen pattern. The allowed patterns are:

- Constant
- Clock
- Random
- Repeater
- Counter

Select Pattern

Signal Name: Edit:/compteur_10/Ck

Start Time: 0 End Time: 100 Time Unit: us

Patterns: Clock Constant Random Repeater Counter

Transcript

```
wave create -pattern none -portmode out -language vhdl -range 3 0 /compteur_10/Q
# compteur_10
VSIM 6>
```

Now: 0 ps Delta: 0 sim:/compteur_10 0 ps to 1 ns

Prise en main de Quartus II



ModelSim ALTERA STARTER EDITION 10.1b

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Library

Name	Type	Path
work	Library	rt_work
compteur_10	Entity	C:/Documents/Altera_Project/compte...
rt_work	Library	C:/Documents/Altera_Project/compte...
220model	Library	\$MODEL_TECH/./altera/vhdl/220model
220model_ver	Library	\$MODEL_TECH/./altera/verilog/220m...
altera	Library	\$MODEL_TECH/./altera/vhdl/altera
altera_insim	Library	\$MODEL_TECH/./altera/vhdl/altera_1...
altera_insim_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_mf	Library	\$MODEL_TECH/./altera/vhdl/altera_mf
altera_mf_ver	Library	\$MODEL_TECH/./altera/verilog/altera...
altera_ver	Library	\$MODEL_TECH/./altera/verilog/altera
altgxb	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_lib	Library	\$MODEL_TECH/./altera/vhdl/altgxb
altgxb_ver	Library	\$MODEL_TECH/./altera/verilog/altgxb
arriagx	Library	\$MODEL_TECH/./altera/vhdl/arriagx
arriagx_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriagx_...
arriagx_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriag...
arriagx_ver	Library	\$MODEL_TECH/./altera/verilog/arriagx
arriaii	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaii_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaii_hssi
arriaii_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaii_p...
arriaii_pcie_hip_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaii_ver	Library	\$MODEL_TECH/./altera/vhdl/arriaii
arriaiigz	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz
arriaiigz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_hssi_ver	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriaiigz...
arriaiigz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriaii...
arriaiigz_ver	Library	\$MODEL_TECH/./altera/verilog/arriaiigz
arriav	Library	\$MODEL_TECH/./altera/vhdl/arriav
arriav_hssi_ver (e...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_pcie_hip_ver...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriav_ver (empty)	Library	\$MODEL_TECH/./altera/verilog/arriav
arriavgz	Library	\$MODEL_TECH/./altera/vhdl/arriavgz
arriavgz_hssi	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_hssi_ver (...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_pcie_hip	Library	\$MODEL_TECH/./altera/vhdl/arriavgz...
arriavgz_pcie_hip_v...	Library	\$MODEL_TECH/./altera/verilog/arriav...
arriavgz_ver (empt...	Library	\$MODEL_TECH/./altera/verilog/arriavgz
cydone	Library	\$MODEL_TECH/./altera/vhdl/cydone
cydone_ver	Library	\$MODEL_TECH/./altera/verilog/cydone

Objects

Name	Value	Kind	Mode
Ck	U	Signal	In
R	U	Signal	In
Q	UUUU	Signal	Out
Qa	UUUU	Signal	Internal

Wave - Default

Msgs	
Edit/compteur_10/Ck	No Data
Edit/compteur_10/R	No Data
Edit/compteur_10/Q	No Data

Specify the Clock Pattern Attributes.

Clock Attributes

Initial Value: 0

Clock Period: 20 ns

Duty Cycle: 50

Transcript

```
wave create -pattern none -portmode out -language vhd1 -range 3 0 /compteur_10/Q
# compteur_10
VSIM 10>
```

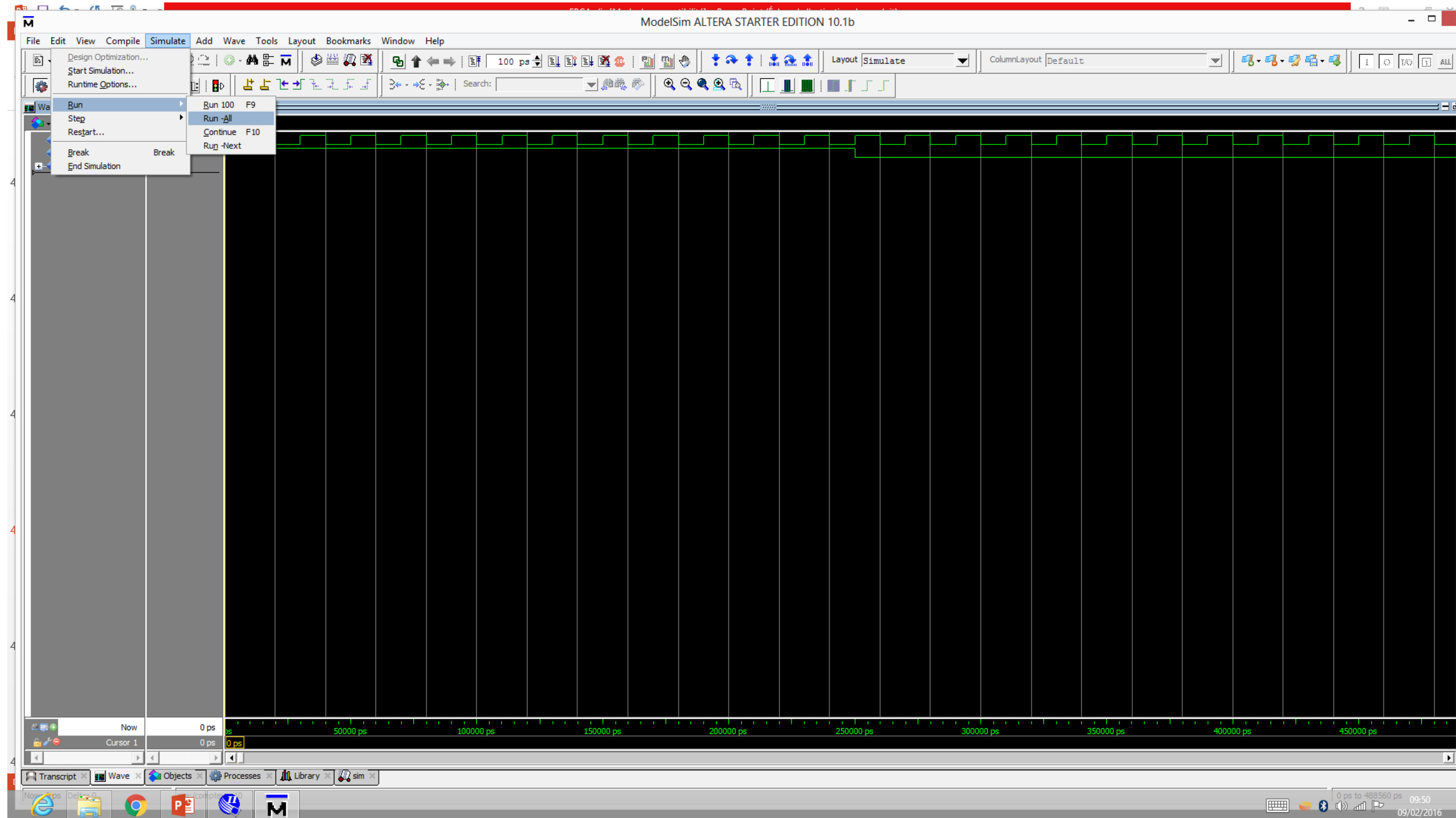
Now: 0 ps Delta: 0

sim:/compteur_10

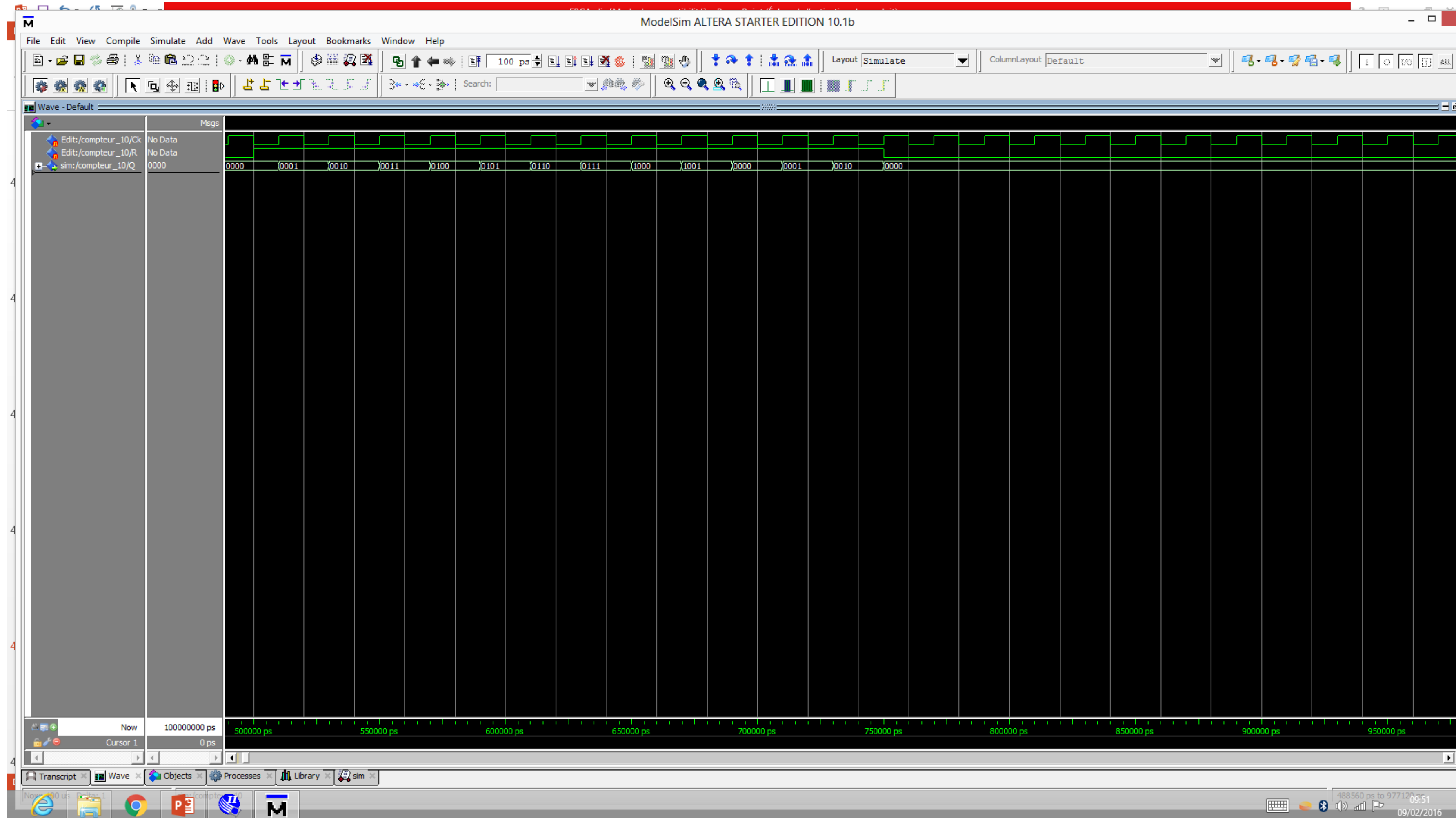
0 ps to 1 ns

09:37 09/02/2016

Prise en main de Quartus II



Prise en main de Quartus II



Prise en main de Quartus II



- Implémentation sur FPGA DEII
 - Assignation des PINs

Signaux	Nom	Pin
Ck	KEY[0]	PIN_G26
R	SW[0]	PIN_N25
Q(0)	LER[0]	PIN_AE23
Q(1)	LER[1]	PIN_AF23
Q(2)	LER[2]	PIN_AB21
Q(3)	LER[3]	PIN_AC22

Prise en main de Quartus II



- Implémentation sur FPGA DE0
 - Assignation des PINs

Signaux	Nom	Pin
Ck	KEY[0]	PIN_J15
R	KEY[1]	PIN_E1
Q(0)	LER[0]	PIN_A15
Q(1)	LER[1]	PIN_A13
Q(2)	LER[2]	PIN_B13
Q(3)	LER[3]	PIN_A11

Prise en main de Quartus II



The screenshot displays the Quartus II IDE interface. The main window shows a VHDL code editor with the following code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

ENTITY Compteur_10 IS
    PORT (Ck, R : IN STD_LOGIC;
          OUT : STD_LOGIC_VECTOR (3 downto 0));
    Compteur_10;
END ENTITY;

ARCHITECTURE Structural OF Compteur_10 IS
    SIGNAL Qa : STD_LOGIC_VECTOR (3 downto 0);
BEGIN
    PROCESS(Ck, R) -- liste de sensibilité
    BEGIN
        IF R = '0' THEN
            Qa <= "0000";
        END IF;
        IF Ck'event AND Ck = '1' THEN -- validation du front montant
            Qa <= STD_LOGIC_VECTOR(UNSIGNED (Qa) + 1);
            IF Qa="1010" THEN Qa <= "0000";
        END IF;
        END IF;
    END PROCESS;
    Q <= Qa;
END Structural;
```

The 'Assignments' menu is open, showing options such as 'Assignment Editor', 'Pin Planner', and 'Timing Closure Floorplan'. The 'Assignment Editor' option is highlighted. The status bar at the bottom indicates 'Ln 26, Col 1' and 'Idle'. The Windows taskbar at the bottom shows several open applications, including 'démarrer', 'Explorat...', '2 quartus', 'Counter2.vh...', 'fpga-rgb-ma...', 'DE2_UserMa...', 'TP_CLM_1.d...', 'Quartus II - ...', 'Circuits sequ...', 'FPGA-dia.pp...', and 'FR'.

Prise en main de Quartus II



The screenshot displays the Quartus II IDE. The main window shows a VHDL code editor for a project named 'Compteur_10'. The code includes library declarations, entity and architecture definitions, and a counter implementation. A status window in the top-left corner shows simulation progress at 100%. An 'Ouvrir' (Open) dialog box is open in the foreground, showing the file explorer for the 'Compteur_10' directory. The file list includes various project files such as reports, summary files, and source files. The 'Compteur_10.qsf' file is selected. The dialog box also shows the file name, file type, and 'Add file to current project' checkbox.

```
1 Library ieee;
2 Use ieee.std_logic_1164.all;
3 Use ieee.numeric_std.all;
4
5 ENTITY Compteur_10 IS
6 PORT (Ck, R : IN STD_LOGIC;
7 Q: OUT STD_LOGIC_VECTOR (3 downto 0));
8 END Compteur_10;
9
10 ARCHITECTURE Structural OF Compteur_10 IS
    -- e sensibilité
    en -- validation du front montant
    GNED (Qa) + 1);
    "0000";
```

Prise en main de Quartus II



This cell specifies the destination name for point-to-point assignments. For single-point assignments, this cell specifies the destination of the assignment. Altera recommends using the Node Finder to assign a destination name.

	To	Assignment Name	Value	Enabled
1	PIN_G26	Location	CK	Yes
2	PIN_N25	Location	R	Yes
3	PIN_AE23	Location	Q(0)	Yes
4	PIN_AF23	Location	Q(1)	Yes
5	PIN_AB21	Location	Q(2)	Yes
6	PIN_AC22	Location	Q(2)	Yes
7	<<new>>	<<new>>		

Info: set_instance_assignment -name PARTITION_HIERARCHY no_file_for_top_partition -to | -section_id Top -remove

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 96 Location: Locate

For Help, press F1

Idle

Prise en main de Quartus II



Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compteur_10.qsf]

File Edit View Project Assignments Processing Tools Window Help

Compteur_10

Module	Progress %	Time
Simulator	100 %	00:00:02

```
27 set_global_assignment -name FAMILY "Cyclone II"
28 set_global_assignment -name TOP_LEVEL_ENTITY Compteur_10
29 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 7.0
30 set_global_assignment -name PROJECT_CREATION_TIME_DATE "19:00:01 FEBRUARY 05, 2016"
31 set_global_assignment -name LAST_QUARTUS_VERSION 7.0
32 set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL "FPGA Compiler II"
33 set_global_assignment -name EDA_INPUT_VCC_NAME VDD -section_id eda_design_synthesis
34 set_global_assignment -name EDA_LMF_FILE fpga_exp.lmf -section_id eda_design_synthesis
35 set_global_assignment -name EDA_INPUT_DATA_FORMAT EDIF -section_id eda_design_synthesis
36 set_global_assignment -name EDA_SIMULATION_TOOL "ModelSim-Altera (VHDL)"
37 set_global_assignment -name EDA_INCLUDE_VHDL_CONFIGURATION_DECLARATION ON -section_id eda_simulation
38 set_global_assignment -name EDA_OUTPUT_DATA_FORMAT VHDL -section_id eda_simulation
39 set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS TEST_BENCH_MODE -section_id eda_simulation
40 set_global_assignment -name EDA_NATIVELINK_SIMULATION_TEST_BENCH TB_Test -section_id eda_simulation
41 set_global_assignment -name EDA_TEST_BENCH_DESIGN_INSTANCE_NAME i1 -section_id eda_simulation
42 set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL "PrimeTime (VHDL)"
43 set_global_assignment -name EDA_INCLUDE_VHDL_CONFIGURATION_DECLARATION ON -section_id eda_timing_analysis
44 set_global_assignment -name EDA_OUTPUT_DATA_FORMAT VHDL -section_id eda_timing_analysis
45 set_global_assignment -name USER_LIBRARIES "C:\\Documents and Settings\\Admin_2\\Bureau\\Lamine\\Matrice_LED_16x32\\rgbmatrici:/
46 set_global_assignment -name DEVICE_FILTER_PIN_COUNT 672
47 set_global_assignment -name VHDL_FILE Compteur_10.vhd
48 set_instance_assignment -name PARTITION_HIERARCHY no_file_for_top_partition -to | -section_id Top
49 set_global_assignment -name PARTITION_NETLIST_TYPE SOURCE -section_id Top
50 set_global_assignment -name VECTOR_WAVEFORM_FILE Compteur_10.vwf
51
52 set_location_assignment Ck -to PIN_G26
53 set_location_assignment R -to PIN_N25
54 set_location_assignment Q(0) -to PIN_AE23
55 set_location_assignment Q(1) -to PIN_AF23
56 set_location_assignment Q(2) -to PIN_AB21
57 set_location_assignment Q(2) -to PIN_AC22
58
```

Warning: Partition name "Top" is reserved -- specify a different name

System Processing Extra Info Info Warning Critical Warning Error Suppressed

Message: 0 of 94 Location: Locate

For Help, press F1 Ln 57, Col 37 Idle

démarrer Explorat... 2 quartus Counter2.vh... fpga-rgb-ma... DE2_UserMa... TP_CLM_1.d... Quartus II - ... 2 Microsoft... Test.qsf - W... FR 20:13

Prise en main de Quartus II



The screenshot displays the Quartus II software interface. The main window shows a compilation report with the following details:

Flow Status	Successful - Fri Feb 05 20:14:50 2016
Quartus II Version	7.0 Build 33 02/05/2007 SJ Web Edition
Revision Name	Compteur_10
Top-level Entity Name	Compteur_10
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	4 / 33,216 (< 1 %)
Total combinational functions	4 / 33,216 (< 1 %)
Dedicated logic registers	4 / 33,216 (< 1 %)
Total registers	4
Total pins	6 / 475 (1 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

The Tools menu is open, showing options such as EDA Simulation Tool, Run EDA Timing Analysis Tool, Launch Design Space Explorer, TimeQuest Timing Analyzer, Advisors, Chip Planner (Floorplan & Chip Editor), Netlist Viewers, SignalTap II Logic Analyzer, In-System Memory Content Editor, Logic Analyzer Interface Editor, SignalProbe Pins..., Programmer (highlighted), MegaWizard Plug-In Manager..., SOPC Builder..., Tcl Scripts..., Customize..., Options..., License Setup..., and Customize Compilation Report....

The Messages window at the bottom shows the following information:

```
Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning
Info: Quartus II Full Compilation was successful. 0 errors, 12 warnings
```

The Windows taskbar at the bottom shows the following open applications: Quartus II, Counter2.vh..., fpga-rgb-ma..., DE2_UserMa..., TP_CLM_1.d..., 2 Microsoft..., and Test.qsf - W... The system tray shows the date and time as 20:23.

Prise en main de Quartus II



The screenshot displays the Quartus II software interface. The main window title is "Quartus II - D:/Altera_Project/Compteur_10/Compteur_10 - Compteur_10 - [Compteur_10.cdf*]". The menu bar includes File, Edit, View, Project, Assignments, Processing, Tools, Window, and Help. The toolbar contains various icons for file operations and project management.

The **Status** window is open, showing the progress of the compilation process. The table below summarizes the progress of each module:

Module	Progress %	Time
Full Compilation	100 %	00:00:
Analysis & Synthesis	100 %	00:00:
Partition Merge	100 %	00:00:
Fitter	100 %	00:00:
Assembler	100 %	00:00:
Classic Timing Analyzer	100 %	00:00:
EDA Netlist Writer	100 %	00:00:

The **Hardware Setup** window is also open, showing the selected hardware: **USB-Blaster [USB-0]** with **Mode: JTAG** and **Progress: 0 %**. A checkbox for "Enable real-time ISP to allow background programming (for MAX II devices)" is checked.

The **Device** window shows the selected device: **Compteur_10.sof** for device **EP2C35F672**. The table below shows the device configuration options:

File	Device	Checksum	Usercode	Program/Configure	Verify	Blank-Check	Examine	Security Bit	Erase	ISP CLAMP
Compteur_10.sof	EP2C35F672	002F87EC	FFFFFFF	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

The **Messages** window at the bottom shows the following information:

- Info: Quartus II EDA Netlist Writer was successful. 0 errors, 1 warning
- Info: Quartus II Full Compilation was successful. 0 errors, 12 warnings

The Windows taskbar at the bottom shows the system tray with the time 20:24 and the language set to FR. The taskbar includes icons for Démarrer, Explorateur, Quartus II, Counter2.vh..., fpga-rgb-ma..., DE2_UserMa..., TP_CLM_1.d..., Quartus II - ..., 2 Microsoft..., and Test.qsf - W...

- Les circuits logiques programmables
- Les circuits FPGA
- Méthodologie de conception des circuits FPGA
- Environnement de développement